High level

- High current, high transient Power Distribution Networks (PDN) need to be able to respond to changes and transients at many different frequencies. Each group of frequencies typically has a different aggressor and a different solution.
Perfect world…

- In this perfect world no capacitors would be needed
Power Supply

• The power supply is not ideal
  – The series resistance and inductance will, however, both typically be very low
  – The output capacitor will have an effective series resistance (ESR) and the leads of the capacitor will have an effective series inductance (ESL)
  – For the capacitor to be effective it should have very low ESR (~10mOhm or better) and a low ESL (see later)
• The PCB is not ideal
  – PCB traces are far from ideal
    • Resistance as low as 10mOhm will cause 40mV drop at 4Amps !!!
    • Long traces, cutouts, thin traces main source of resistance
    • Vias, thin traces main source of inductance
  – Resistance causes variation in device voltage due to changes in load current
  – Inductance causes variation in device voltage due to changes in load current frequency characteristics
Decoupling

• Decoupling is supposed to provide short term support for the supply
  – Bulk capacitors support low frequency changes (MHz)
  – Ceramic decaps support mid to high frequency changes (10s to 50s+ MHz)
  – Inter-plane capacitance supports high frequency changes (200MHz+)
  – On die capacitance supports high frequency changes (400MHz+)
  – Forms filter with PCB trace RL and series RLC
Package Leads

- Package leads introduce more series resistance and inductance
- Wire bond devices have additional inductance compared to flip chip
- BGA packages tend to have lower RL compared to leaded packages
Package Capacitance

- Package will have ‘stray’ capacitance and possibly additional intentional capacitance.
  - Inductance usually very low
  - Resistance should be low
  - Capacitance also low
  - Helps with very high frequency (400MHz+)
• On die power distribution will have resistance and inductance
• Capacitance may also be added in some devices
Capacitor Characteristics

- Impedance of capacitor is frequency dependent
- Low frequency governed by capacitor value
- High frequency governed by inductance of leads and mounting
- If widely spaced self resonance then can oscillate/resonate
Reduce Inductance

• Reducing inductance is one of the most critical aspects of PDN
  – Capacitor geometry
    • 1210, 0805, 0603, 0402. Smaller = better
    • Long & thin vs short & fat, multi-terminal
  – Capacitor connectivity

![Diagrams showing capacitor geometry and connectivity](image-url)
How Capacitors Help

• Provide short term local power during changes in supply current
• Have little effect at frequencies above or below self resonance frequency
• Multiple capacitors needed to ensure required impedance across all critical frequencies
Time Domain Analysis

• Large value capacitors tend to have large inductance
  – Can provide support for slower changing demands and for longer periods of time
  – Cannot provide rapid response to quick changes due to inductance

• Small value capacitors tend to have small inductance
  – Can respond to quick changes but only for short periods of time
  – Cannot provide support for slow changing demands due to low C values
**Step Response in Current**

- At a step change in current draw (red) the voltage at the device (green) will drop. With no decoupling the voltage will continue to drop until the power supply can provide the additional current. Board inductance means that there will be time before this occurs.

- Local decaps provide short term support but cap inductance still delays the response (blue)
Capacitor Response

1. Change in current requirements
2. Voltage drops due to increased I demand
3. Decap supplies current after inductance caused delay
4. Decap discharges hence can no longer help as much
5. Power supply (and distribution) begins to respond
6. Power supply fully recovered

- Red = current
- Green = No decap
- Blue = With decap
Frequency Components

- Many different sources of step current change exist in a real system
  - DDR activity
    - Burst activity in MHz to 100s MHz range
    - Transaction level in 800MHz range
  - CPU/DSP activity changes
    - Enable/disable features in seconds range
    - Coprocessor activity bursts in MHz range
  - Internal connectivity
    - L1/L2/L3 bursts and transactions
  - Other peripherals
    - Serial ports
    - USB
    - Ethernet
- Each of these additionally has an edge rate with harmonics
Static Change in Current

• When the processing load changes then there can be a static change in the load current
  – E.g. switch from 1 channel to 16 channels

• After the step change in current there will then also be a change in the device voltage caused by the PCB resistance

• Correctly placed PS feedback should correct for this change in voltage but it will take time for load voltage to actually correct

• Smart Reflex might also be able to correct this but with a much slower response time
Target Impedance

• In order to ensure that the voltage at the device balls does not violate the required Vmin it is necessary to ensure that the PCB impedance across all significant frequencies does not fall below some value
  – From Ohms law we know $R = \frac{V}{I}$
    • Where $R =$ resistance, $V =$ voltage drop and $I =$ current
  – Therefore, for a step current change of $I_{\text{delta}}$ we will see a voltage change of $V_{\text{delta}}$ at a frequency of $w$ caused by the board impedance $Z_w$
Z Target Calculation

\[ Z_{\text{target}} = V_{\text{supply}} \times V_{\text{tolerance}} / I_{\delta} \]

• NB some people prefer to use \( I_{\text{max}} \) rather than \( I_{\delta} \) to account for static IR drop. Necessary if feedback not implemented

• \( Z_{\text{target}} \) = Maximum PCB impedance allowed
• \( V_{\text{supply}} \) = Required voltage
• \( V_{\text{tolerance}} \) = % allowed error/tolerance
• \( I_{\delta} \) = Maximum expected/measured step current step/change
Must Meet $Z_{target}$

- Spreading the 100nF across a wider range will reduce peaking.
- Ex: 1uF, 560nF, 220nF, 100nF, 47nf
**$Z_{\text{target}}$ requirements**

- A step change in current will contain energy components at all frequencies hence $Z_{\text{target}}$ must be maintained at all frequencies.
- Different capacitors reduce the impedance at different frequencies.
- When combined the impedance contributors must yield an impedance below $Z_{\text{target}}$ at all frequencies (see example above, red line = $Z_{\text{target}}$, green dotted line = achieved impedance with selected capacitors and board characteristics).
- No individual capacitor achieved acceptable result but combined impedance is below required i.e. good.
Historically...

- Historically simply adding 0.1uF caps worked
  - Why did it work (mostly)?
    - Not concerned with high frequencies, only C was important
    - Currents typically smaller, higher impedance OK
    - Voltages typically higher, more noise OK

![Diagram showing the relationship between impedance (Z) and frequency (f)]. Adding more C pushes the impedance down until it meets the goal.
“Big V” Does not work anymore…

• More care needs to be taken now
  – Why does it not work now?
    • Higher frequencies, L now important
    • Currents typically higher, target Z lower
    • Voltages typically lower, noise not OK (needs lower Z too)

Need to target different frequency components more selectively now to avoid over design at mid frequencies.
Target L & C for optimal results

- Different C in same package/connection etc…

In reality inductance is different too. Inductance not directly affected by capacitance value but may be different due to other effects e.g. package.

Smaller package usually lower ESL.
Lower C and lower ESL moves resonance frequency up.
Target L & C for optimal results

- Multiple capacitors in parallel to make up same C give lower L
Real life target $Z$

- In reality high frequencies handled by the die & package so target $Z$ relaxed at higher frequencies

- Above $f_{\text{cut-off}}$ board design not critical
Real life target $Z$

- Assumed $I_{\text{delta}}$ constant at all frequencies so far
  - In reality max frequency is application dependent
  - Lower current at higher frequencies allows higher $Z$

- Between $f_{\text{dynamic}}$ and $f_{\text{cut-off}}$ requirements relaxed but care needs to be taken
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