High Power, Low Noise Power PCB Design

Things to do in order to achieve reliable high current power supply distribution in low voltage processor designs

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Requirements

In high current processor systems stable power supply and distribution is critical.

Old design methodologies of just adding 0.1uF and 0.01uF caps no longer work.

PCB layout, stack-up and component packaging now critical due to high frequency demands on the power supply and distribution.

What we want

What we get
Free Inductor With Every Capacitor

Whilst it is slowly becoming better understood that the “Big V” approach to power supply design is not sufficient it is often difficult to know how to ‘fix it’.

![Graph showing impedance due to decoupling capacitors with frequency components]

Need to target different frequency components more selectively now to avoid over design at mid frequencies. Need to ensure other factors in the design do not negate capacitor usefulness.
End Game

The ultimate requirement of the power distribution network (PDN) is to ensure a low impedance supply from the voltage regulator module (VRM) to all target device power supply pins at all important frequencies.

‘Fdynamic’ is the maximum frequency at which the system can generate demand and is application dependent.

‘Fcutoff’ is the frequency at which the package and die take over and the PCB design has little impact*1.

‘Target Impedance’ is the impedance required to ensure the voltage at the processor will not drop below the required level.

*1 PCB will still interact with package and die to affect the resonant frequency.
Hitting The Target

Reducing the impedance between the power supply (VRM) and the device is important, but what does it really need to be?

Since impedance is a frequency dependent parameter what does the impedance need to be and over what frequency range?

The target impedance depends on the peak delta in current requirements, the application activity frequency determined by the device (note this is not the clock frequency) and the device package and die characteristics.

At some point (termed Fcutoff) the package inductance and die capacitance will become dominant and the capacitors & PCB characteristics become inefficient.

At low frequencies (< 10’s KHz) the VRM itself will be dominant.

The device will not make demands at all frequencies equally and at some frequency (termed Fdynamic) the system impedance requirements start to diminish.
Relax... A Graduated Target Impedance (GTI) Methodology

Review of a board design completed with flat $Z_t$ shows >50% of capacitors targeted at frequencies above 20MHz ($F_{knee}$).

Capacitor quantity is lower and placement proximity requirements more relaxed for caps below $F_{knee}$. Thus, cheaper and easier to “overdesign” below $F_{knee}$.

Current Guidelines:

- $Z_{t-L} = (V_{tol-AC} \times 0.5)/I_{delta}$
- $Z_{t-H} = V_{tol-AC}/I_{delta}$
- $F_{cutoff}$: Max effective frequency for board bypass caps (driven by package and board parasitics)
Impedance Is The Key

The key to being able to reduce the impedance of a power distribution network is to reduce the inductance and resistance between the power source and the power sink, and adding capacitance to compensate for deficiencies.

In a perfect system, if the power distribution impedance is zero then there is no need for any decoupling capacitors. Real life is not this nice though.

Even solid planes have resistance and will introduce inductance (there is still a loop created).

There will always be package inductance in series with die capacitance which will resonate with the PCB. This resonance needs to be above the highest dynamic frequency and above the cutoff frequency if possible.
De-Loop De Loop

Inductance is proportional to loop area.

Inductive loops created when connecting a top side capacitor through top level power planes.

Inductive loops created when connecting a top side capacitor through lower level power planes.

Inductive loops created when connecting a bottom side capacitor with via in pad connections.

- Sometimes smaller loops can be achieved by using top side capacitors close to the processor if space and routing permit.
- The thicker the board the less effective back side caps will be.
- The closer the power plane to the die the more effective top side caps will be.
Simple Stuff First

Reducing the resistance of connections not only reduces the DC resistance (hence voltage drop) but will reduce the effective inductance caused by current crowding.

Flood fill as many power related regions as possible.

Many pads are connected through a single, small trace. This causes high resistance and high inductance. Even in regions where there are multiple connections it is still not utilizing the space to provide the lowest impedance possible.

Multiple vias on same net, but connection only made to one. Flood these regions for lower impedance connections.

Solid floods allow the simplest and quickest way to utilize as much copper as possible whilst still meeting clearance and design rules. PWR/GND vias still spaced too much though in this example.
More Is (Usually) Better

In addition to adding as much copper as possible it is critical to connect islands as quickly and often as possible to their corresponding planes.

Add as many vias as possible on all ground and power floods.

Having said this... It is sometimes better to sacrifice a capacitor to allow the ground and power vias to be placed closer together, reducing the loop area hence the inductance.

Removing one or more capacitors will allow these and other via pairs to be moved much closer together. Closer via pairs can be better than more vias/capacitors.
Less Is Better

When adding vias, place ground and power vias as close as possible together. Inductance is a function of the loop area so reducing the loop area will reduce the effective inductance.

Vias on the side of capacitors create smaller loops than vias on the ends of capacitors.

Capacitors on the layer closest to the power/ground planes create smaller loops than capacitors far from the power/ground planes and have shorter via stubs.
Smaller is Better

Capacitor package choice and connection style is critical if the capacitor is to be useful at all. Badly chosen capacitors and/or connection can actually cause resonance peaks rather than the desired overall low impedance.

Smaller packages typically have lower lead inductance and allow closer via placement resulting in lower loop inductance.
Closer Is Better

The closer power and ground planes are together then the lower the impedance will be, and higher the inter-planar capacitance. The layers should also be as close as possible to the processor in the stackup, again reducing the inductance and resistance through vias. Previously mentioned power/ground flood fills wherever possible also help introduce planar capacitance.
Starting Point

The package and die of the processor will have an implicit impedance profile which cannot be changed by PCB layout and determine the lowest impedance of the final design. Care needs to be taken to ensure that PCB & die and package resonance is above Fcutoff.

A processor die & package impedance profile might look something like the profile to the left. It is very difficult to add PCB capacitance which is effective at frequencies close to this hence in most cases these higher frequencies must be handled by the die and package directly.
Low Point

The voltage regulator module (VRM) will also have an impedance profile which will be effective at the lower frequencies. The VRM is simply the voltage regulator and/or power supply switcher circuit.

Note, the VRM switching capacitors should not be considered low frequency (bulk) capacitance. Bulk capacitors should be placed closer to the processor and serve a different purpose.
Regions Of Interest

There are basically four regions of interest. Each region has its own impedance requirements and its own solution.

A) VRM dominates.
B) Bulk and decoupling capacitors effective and |Z| requirements tighter.
C) Decoupling capacitors less effective and |Z| requirements relaxed.
D) Decoupling capacitors ineffective. Package inductance and die capacitance dominant.
What Is The Target

If the power distribution network (PDN) does not have a sufficiently low impedance across all critical frequencies then in will behave as though there is a series resistance at some frequencies. This resistance (really the impedance) will mean there is a voltage drop when excited at the culprit frequency.

Therefore it is necessary to understand the impedance ‘plot’ which shows the PDN impedance across frequencies of interest.

Impedance profile of 10x typical 0.1uF capacitors in parallel with 10x 0.01uF capacitors
Overshooting The Target

Just picking ‘random’ capacitors does not always help (usually does not help)

In this example, once the package and die characteristics are included we can see that these particular 0.01uF capacitors are effective at exactly the same frequency as the package/die is already working, hence the 0.01uF capacitors to not help much. The impedance is already low enough at the effective frequency.

Also note that the resultant impedance INCREASES in some regions due to inter-component resonance. In this case, the die capacitance is resonating with the 0.1uF capacitor’s self-inductance. This is why more is not always better.
Inter component resonance can make things significantly worse if care is not taken choosing capacitor values, capacitor packages, connection styles and routing.

Capacitor/capacitor/package/die resonance causes significant peaks in this example which results in an impedance which is significantly higher than just the components would be on their own. The expectation would normally be for the impedance to be lower than the capacitors on their own but it isn’t.
Moving Target

The target impedance therefore depends on the device power supply requirements (% tolerance) and expected change in current requirements during operation.

Using Ohm’s law a good rule of thumb is...

\[ R = \frac{V}{I} \]

Which transposes to...

\[ |Z| \sim \frac{\Delta V}{\Delta I} \]

Where...

\[ \Delta V = \text{max allowable delta in supply voltage} \]
\[ \Delta I = \text{max ‘instantaneous’ delta in device supply current} \]

Note, the max allowable delta in voltage will be smaller than the specified voltage tolerance in the device datasheet and must take into account all system tolerances such as resistor values etc...
The above calculations assume no resonance is introduced and that capacitors also do not introduce any resonance (very simple, first order estimate).

Resonance will be introduced when capacitances and inductances interact with each other, particularly with the package and die. Resonance will cause the effective impedance to go up.

In order to allow the use of simple tools the target impedance should include additional margin. A good rule of thumb is to de-rate the target impedance by a factor of 1/2x below Fcutoff. This will end up over designing in some frequency regions but hopefully ensure adequately low impedance targets at all critical frequencies.

For processors a good rule of thumb for ‘application activity frequency’ is Fosc/16. This is determined empirically and is the number of system clocks to switch from sleep to fully active, for example.
Smooth Operator

Once the target impedance is determined you can then work on attaining it with capacitor selections and placement.

The resultant impedance profile should be as smooth as possible and not include any large resonant peaks in impedance. Peaks will cause the impedance calculations to be sensitive to small errors in mounting/board inductance estimations.
Introduce Some Variety

Traditionally decoupling solutions have consisted of adding 0.1uF and 0.01uF capacitors. Unfortunately this simply creates a ‘Big V’ impedance profile. A better (and necessary) approach is to target capacitors to quell high impedances at specific frequencies. Different capacitors have different lead inductances. Including different connection styles, packages and placements will drastically change the effective impedance.
Checklist

With some fairly simple steps the integrity of power supply distribution can be improved and made more robust. It is still recommended to perform a detailed analysis of any PDN but the following steps will set you in the right direction, making fine tuning later much simpler.

1) Flood all areas possible
2) Add as many vias as possible without ‘Swiss cheese” critical planes
3) Reduce/eliminate via sharing
4) Place power and ground vias as close as possible
5) Ensure full ground and power planes and as close as possible together and to the target device
6) Use thickest possible copper foil for power and ground layers
7) Use 0402 or smaller capacitor packages
8) Minimize capacitor connection stub lengths
9) Use capacitor values and styles to meet broad spectrum impedance requirements (Use PDN XLS as a guide)
10) Validate as accurately as possible. (2.5D** and 3D solver simulation)

**Some 2.5D simulators do not model via inductances very well and can result in very inaccurate results. Full 3D solvers are preferred.
Case Study

Utilizing these strategies the following improvements were made on a custom design.

Impedance reduced from over 100mΩ to about 50mΩ.
Peak impedance effective frequency increased by 12MHz.
Impedance reduced for most frequencies in region of interest.
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Power Up article

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