AM572x SR1.1 to SR2.0 Migration

Hardware changes

- Updated CTRL_WKUP_ID_CODE[31:28] VERSION to allow for software to distinguish between silicon revisions.ID
- The internal PU/PD resistors on pads gpmc_a[27:19]/mmc2_dat[7:0] can be permanently disabled. For more information, see Section 18.4.6.1.1.1, Permanent PU/PD disabling (SR2.0 only) of the AM572x TRM.
- RGMII internal transmit delay can be disabled via CTRL_CORE_SMA_SW_1.
- ICSS updates
  - CRC16/32 module
  - Increase IEP Timer compare registers from 8 to 16
  - IEP Timer updated from 32-bit timer to 64-bit timer. Register set is backward compatible.
- New manual IO timing in the data manual.
- VD_CORE boot voltage: For best compatibility, a boot voltage of 1.15V will work on both silicon revisions.
  - SR1.1 allows a nominal boot voltage of 1.15V or 1.06V.
  - SR2.0 allows a nominal boot voltage of 1.15V only.
- VD_MPU boot voltage: For best compatibility, a boot voltage of 1.15V will work on both silicon revisions.
  - SR1.1 allows a nominal boot voltage of 1.15V or 1.10V.
  - SR2.0 allows a nominal boot voltage of 1.15V only.
- sysboot15 behavior: This affects the internal pull-down (IPD) related to the mmc2_dat[7:0] signals.
  - SR1.1 requires sysboot15 tied high. The mmc2_dat[7:0] signals always have a weak pull-down enabled at boot as described in erratum i863.
  - SR2.0 the pin behaves as follows:
    - SYSBOOT15 = 0 (IPD enabled)
      - Systems booting from GPMC (e.g. parallel NOR boot) should use this configuration in order to keep the corresponding GPMC address pins low during boot.
    - SYSBOOT15 = 1 (IPU/IPD permanently disabled)
      - Systems booting from MMC2 (e.g. eMMC) should use this mode, which resolves the issue of the contention of i863
  - For complete details, please see the TRM Section 18.4.6.1.1.1 "Permanent PU/PD disabling (SR 2.0 only)".

Errata fixes

- i843: MMC1/2/3 Speed Issues
- i863: MMC2 Has PU/PD Contention Immediately after Release from Reset
- i868: McASP to EDMA Synchronization Level Event Can Be Lost
- i875: Power-on-Reset (PORz) Warm Boot Hang
- i880: Ethernet RGMII2 Limited to 10/100 Mbps (SR2.0 status pending IO timing characterization)
- i882: EMIF: DDR ECC Corrupted Read/Write Status Response
- i884: MMC4 Speed Limited to 38.5 MHz

Software

- Processor SDK 2.00.02 and later will support SR2.0

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